Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please add new claims 73-92 as follows:

Listing of Claims:

Claims 1-72 (Canceled)

Canceled

~~73.~~ (New) A data path for coupling data between a memory array and a plurality of data bus terminals, the data path comprising:

M*N flip-flops coupled to the memory array to receive respective read data bits from the memory array;

an M*N-bit data bus coupled to the M*N flip-flops;

a first set of N parallel-to-serial converters coupled to the M*N-bit data bus, each of the parallel-to-serial converters in the first set being operable to receive either M or M/2 parallel data bits from the M*N flip-flops, to convert the M or M/2, respectively, parallel data bits to M or M/2, respectively, serial data bits, and to couple the M or M/2, respectively, serial data bits to a respective one of N data bus terminals;

a second set of N parallel-to-serial converters coupled to the M*N-bit data bus, each of the parallel-to-serial converters in the second set being operable to receive M/2 parallel data bits from the flip-flops, to convert the M/2 parallel data bits to M/2 serial data bits, and to couple the M/2 serial data bits to a respective one of N data bus terminals; and

a control circuit operable in a first operating mode to cause M*N bits of data from the M*N flip-flops to be coupled through the M*N-bit bus in parallel and to cause M of the parallel data bits to be coupled to each of the N parallel-to-serial converters in the first set, and being operable in a second operating mode to cause M*N bits of data from the M*N flip-flops to be coupled through the M*N-bit bus in parallel and to cause M/2 of the parallel data bits to be coupled to each of the N parallel-to-serial converters in the first set and to each of the N parallel-to-serial converters in the second set.

Canceled

74. (New) The data path of claim 73 wherein M is equal to 8 and N is equal to 8.

75. (New) The data path of claim 73 wherein the memory array comprises first and second sub-arrays, and wherein the M*N flip-flops comprise a first set of M*N/2 flip-flops coupled to the first sub-array and a second set of M*N/2 flip-flops coupled to the second sub-array.

76. (New) A data path for coupling data between first and second memory arrays and 16 data bus terminals, the data path comprising:

two sets of 32 flip-flops coupled to each of the memory arrays, respectively, each of the flip-flops receiving a respective read data bit from the memory arrays;

a 32-bit data bus coupled to each set of flip-flops;

a first set of 4 parallel-to-serial converters coupled to each of the 32-bit data buses, each of the parallel-to-serial converters in the first set being operable to receive either 8 parallel data bits or 2 sets of 4 parallel data bits from the 64 flip-flops, to convert the parallel data bits to 8 serial data bits, and to couple the 8 serial data bits to a respective one of 8 data bus terminals;

a second set of 4 parallel-to-serial converters coupled to each of the 32-bit data buses, each of the parallel-to-serial converters in the second set being operable to receive 2 sets of 4 parallel data bits from the 64 flip-flops, to convert the parallel data bits to 8 serial data bits, and to couple the 8 serial data bits to a respective one of 8 data bus terminals; and

a control circuit operable in a first operating mode to cause 32 bits of data from the 32 flip-flops in each set to be coupled through the respective 32-bit data bus and to cause 8 of the data bits to be coupled to each of the 4 parallel-to-serial converters in each of the first sets, and being operable in a second operating mode to first cause a first group of 32 bits of data from the 32 flip-flops in each set to be coupled through the respective 32-bit bus and to cause 4 of the data bits in the first group to be coupled to each of the 4 parallel-to-serial converters in each of the first sets and 4 of the data bits to be coupled to each of the 4 parallel-to-serial converters in

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each of the second sets and to then cause a second group of 32 bits of data from the 32 flip-flops in each set to be coupled through the respective 32-bit bus and to cause 4 of the data bits in the second group to be coupled to each of the 4 parallel-to-serial converters in each of the first sets and 4 of the data bits in the second group to be coupled to each of the 4 parallel-to-serial converters in each of the second sets.

claims renumbered

1 77. (New) A method of transferring data to or from a memory device in either a first operating mode or a second operating mode, the method comprising:

in the first operating mode, transferring data to or from 2N data bus terminals of the memory device in form of a burst of M bits of data to or from each terminal; and

in the second operating mode, transferring data to or from N data bus terminals of the memory device in form of a burst of M bits of data to or from each terminal.

2 78. (New) The method of claim 77 wherein the acts of transferring data to or from the data bus terminals comprise transferring data from the data bus terminals in a data read operation.

3 79. (New) The method of claim 78 wherein the act of transferring data to or from 2N data bus terminals of the memory device in form of a burst of M bits of data to or from each terminal comprises:

transferring a first set of M*N data bits from a memory array in a first read operation;

storing the read M*N data bits;

transferring a second set of M*N data bits from the memory array in a second read operation; and

sequentially transferring M bits of the stored M*N data bits and the M data bits in the second set of M*N data bits from each of the 2N data bus terminals.

80. (New) The method of claim 79 wherein the acts of transferring a first set of M*N data bits from a memory array in a first read operation and transferring a second set of M*N data bits from the memory array in a second read operation comprise transferring M*N bits from the memory array in parallel in each of the first and second read operations.

81. (New) The method of claim 78 wherein the act of transferring data to or from N data bus terminals of the memory device in form of a burst of M bits of data to or from each terminal comprises:

transferring a M*N data bits from a memory array in a read operation;

sequentially transferring M bits from each of the N data bus terminals.

82. (New) The method of claim 81 wherein the act of transferring M*N data bits from a memory array in a read operation comprises transferring M*N bits from the memory array in parallel during the read operation.

83. (New) The method of claim 78 wherein the act of transferring data to or from 2N data bus terminals of the memory device in form of a burst of M bits of data to or from each terminal comprises:

transferring a first set of M/2 parallel data bits from a memory array for each of the 2N data bus terminals;

transferring a second set of M/2 parallel data bits from the memory array for each of the 2N data bus terminals;

converting the transferred first and second sets of M/2 parallel data bits to M serial data bits for each of the 2N data bus terminals; and

coupling the M serial data bits from each of the 2N data bus terminals.

84. (New) The method of claim 78 wherein the act of transferring data to or from N data bus terminals of the memory device in form of a burst of M bits of data to or from each terminal comprises:

transferring M parallel data bits from a memory array for each of the N data bus terminals;

converting the transferred M parallel data bits to M serial data bits for each of the N data bus terminals; and

coupling each of the M serial data bits from each of the N data bus terminals.

9 85. (New) The method of claim 77 wherein N is equal to 8 and M is equal to 8.

10 86. (New) The method of claim 77 wherein the acts of transferring data to or from the data bus terminals comprise transferring data to the data bus terminals in a data write operation.

11 87. (New) The method of claim 86 wherein the act of transferring data to or from 2N data bus terminals of the memory device in form of a burst of M bits of data to or from each terminal comprises:

sequentially transferring M bits of data to each of the 2N data bus terminals.

transferring a first set of M*N data bits to a memory array in a first write operation;

transferring a second set of M*N data bits to the memory array in a second write operation.

12 88. (New) The method of claim 87 wherein the acts of transferring a first set of M*N data bits to a memory array in a first write operation and transferring a second set of M*N data bits to the memory array in a second write operation comprise transferring M*N bits to the memory array in parallel in each of the first and second write operations.

13 89. (New) The method of claim 86 wherein the act of transferring data to or from N data bus terminals of the memory device in form of a burst of M bits of data to or from each terminal comprises:

sequentially transferring M bits to each of the N data bus terminals.

transferring a M*N data bits to a memory array in a write operation;

14 90. (New) The method of claim 89 wherein the act of transferring M*N data bits to a memory array in a write operation comprises transferring M*N bits to the memory array in parallel in the write operation.

15 91. (New) The method of claim 86 wherein the act of transferring data to or from 2N data bus terminals of the memory device in form of a burst of M bits of data to or from each terminal comprises:

coupling M serial data bits to each of the 2N data bus terminals;

converting the M serial data bits for each of the 2N data bus terminals to first and second sets of M/2 parallel data bits;

transferring the first set of M/2 parallel data bits to a memory array for each of the 2N data bus terminals; and

transferring the second set of M/2 parallel data bits for each of the 2N data bus terminals to the memory array.

16 92. (New) The method of claim 86 wherein the act of transferring data to or from N data bus terminals of the memory device in form of a burst of M bits of data to or from each terminal comprises:

coupling M serial data bits to each of the N data bus terminals;

converting the transferred M serial data bits to M parallel data bits for each of the N data bus terminals; and

transferring the M parallel data bits for each of the N data bus terminals to a memory array.